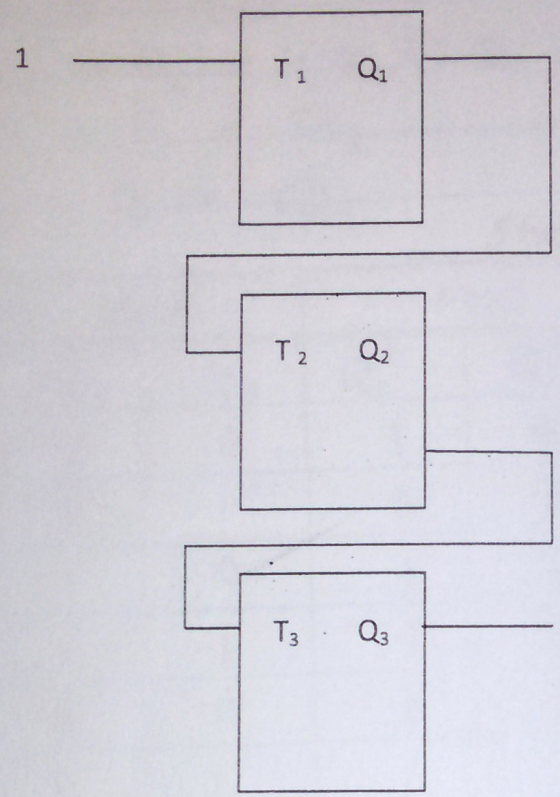
Mid Term Exam | Computers and Systems Dept.

System Design | Time allowed: 1hr

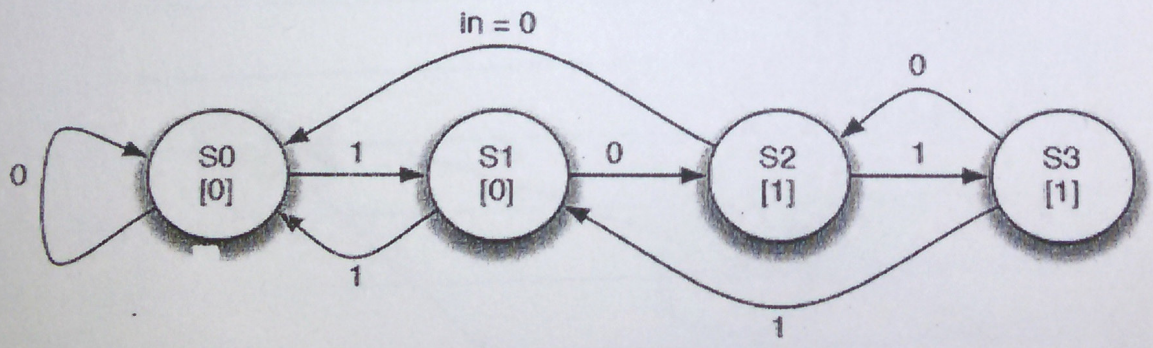
Question 1:

Analyze the following circuit:



Question 2:

Design sequential circuit that follows the following state diagram using JK flip flops. Notice that the output is written inside the circle.



Question 3:

Write the VHDL code that simulates the circuit in two methods behavioral and hierarchical:

F = X.Y.Z + X xor Z xor Y

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Digital Systems

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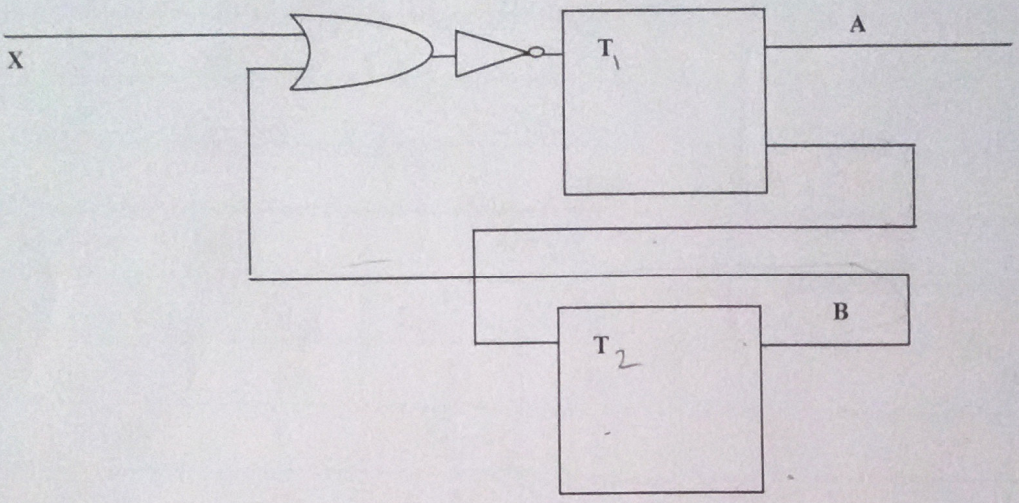
Total (20 degrees)

Question 1: (4 degrees)

Analyze the following circuit shown in figure.



Question 2: (5 degrees)

Design a sequential circuit that has 4 states: fetch, decode, execute and save. It works as follows:
1- The fetch state fetches either an operation or data. If it is data, the second state is skipped and the execute state is called.
2- In the execute state, if it is a data the save state is next. However, if it is operand the data must be fetched by going back to the fetch state.
3- The decode goes directly to execute and the save goes back to the fetch state.

Draw the state diagram of the circuit first, then make the design and finally draw the circuit.

Question 3: (4 degrees)

State true and false then explain it in brief:
1- The JK flip flop excitation table can not be predicted.
2- The state reduction is not important and does not affect the circuit.

Question 4: (7 degrees)

Write down the VHDL code for a circuit that follows the following diagram (do not describe the behavior of counter, just the decoder).
Bonus (2 degrees) state how this circuit works.